Amendments to the Claims:

1. (Currently Amended) An integrated circuit comprising:

a memory,

a digital signal processor coupled to said memory,

first and second direct memory access devices each coupled to said memory, said first and second direct memory devices adapted to receive data from a first external device;

an interface device coupled to said memory and adapted to receive data from a second external device; ~~and~~

a first sharing unit coupled to said memory and to said first and second direct memory access devices and adapted to alternately couple said first and said second direct memory access devices to said memory; and

a second sharing unit coupled to said memory, to said first sharing unit and to said interface device, said second sharing unit adapted to alternately couple said first sharing unit and said interface device to said memory.

2. (Original) The integrated circuit of Claim 1, wherein:

said first and second direct memory access devices are programmable logic cores.

3. (Original) The integrated circuit of Claim 1, wherein:

said digital signal processor operates at a first clock frequency,

said first and second direct memory access devices operate at a second clock frequency slower than said first clock frequency.

4. (Original) The integrated circuit of Claim 3, wherein:

said second clock frequency is one-fourth of said first clock frequency and said first sharing unit alternates connection of said first and second direct memory access devices to said memory at a frequency of one-half of said first clock frequency.

5. (Original) An integrated circuit according to Claim 4, wherein:

said first clock frequency is 160 megahertz.

6. (Original) The integrated circuit of Claim 1, further comprising:

a memory controller coupled to said memory, to said digital signal processor and to said first sharing unit,

said memory controller adapted to, in response to a memory transaction request from a direct memory access device, provide a control signal indicating that the requested operation was done if there was no conflicting request from said digital signal processor and provide a control signal indicating that the requested operation was not done if there was a conflicting request from said digital signal processor.

7. Canceled.

8. (Currently Amended) The integrated circuit of Claim ~~7~~ 1, wherein:

said digital signal processor operates at a first clock frequency,

said ~~third direct memory access~~ interface device operates at a second clock frequency slower than said first clock frequency,

said first and second direct memory access devices operate at a third clock frequency slower than said second clock frequency.

9. (Currently Amended) The integrated circuit of Claim 8 wherein:

said second clock frequency is one-half said first clock frequency,

said third clock frequency is one-fourth of said first clock frequency,

said first sharing unit alternates connection of said first and second direct memory access devices to second sharing unit at a frequency of one-half of said first clock frequency, and

said second sharing unit alternates connection of said first sharing unit and said ~~third direct memory access~~ interface device to said memory at said first clock frequency.

10. (Original) An integrated circuit according to Claim 9, wherein:

said first clock frequency is 160 megahertz.

11. (Currently Amended) An integrated circuit comprising:

a digital signal processor operating at a first clock frequency and having an internal memory,

a first direct memory access device adapted to received data from a first external device, said first direct memory device operating at a second clock frequency slower than said first clock frequency;

a second direct memory access device adapted to receive data from said first external device, said second direct memory device operating at a third clock frequency slower than said first clock frequency;

an interface device adapted to receive data from a second external device, said interface device operating at a fourth clock frequency slower than said first clock frequency;

a first sharing unit having a first port coupled to the first direct memory access device, a second port coupled to the second direct memory access device, and a third port coupled to the digital signal processor internal memory, said first and second ports alternately coupled to said third port in synchronization with said first clock frequency; and

a second sharing unit having a first port coupled to the first sharing unit third port, a second port coupled to the interface device, and a third port coupled to the digital signal processor internal memory, one of said second sharing unit first and second ports alternately coupled to said second sharing unit third port in synchronization with said first clock frequency.

12. Canceled.

13. (Original) An integrated circuit according to Claim 11, wherein:

each of said first and second direct memory access devices is a programmable logic core.

14. Canceled.

15. (Currently Amended) An integrated circuit according to Claim ~~14~~ 11, wherein:

said fourth clock frequency is one half said first clock frequency,

said second clock frequency and said third clock frequency are each one-fourth of said first clock frequency,

said first sharing unit alternates connection of its first and second ports to its third port at a frequency of one-half of said first clock frequency, and

said second sharing unit alternates connection of its first and second ports to its third port at a frequency equal to said first clock frequency.

16. (Original) An integrated circuit according to Claim 15, wherein:

said first clock frequency is 160 megahertz.

17. Canceled.

18. (Original) An integrated circuit according to Claim 11, wherein:

said digital signal processor comprises a processor core, a memory and a memory controller,

said memory controller couples memory operations between said processor core and said memory and between said direct memory devices and said memory,

said memory controller, in response to a memory transaction request from a direct memory access device, provides a control signal indicating that the requested operation was done if there was no conflicting request from the processor core and provides a control signal indicating that the requested operation was not done if there was a conflicting request from the processor core.

19. Canceled.

20. Canceled.

21. (New) An integrated circuit comprising:

a bus subsystem adapted for coupling to a first external device;

a bus interface coupled to said bus subsystem;

a programmable logic core adapted for coupling to a second external device;

a digital signal processor subsystem; and

a sharing unit coupled to said bus interface and said programmable logic core, said first sharing unit adapted to alternately couple said bus subsystem and said programmable logic core to said digital signal processor subsystem.

22. (New) An integrated circuit according to claim 21, wherein said first external device is configured to transfer data to said digital signal processor subsystem via said bus interface and said second external device is configured to transfer data to said digital signal processor subsystem via said programmable logic core.

23. (New) An integrated circuit according to claim 21, wherein said bus subsystem further comprises:

a first bus section; and

a second bus section coupled to said first bus section

said first bus section adapted for coupling to said first external device and said second bus section adapted for coupling to said second external device.

24. (New) An integrated circuit according to claim 23, wherein:

said first bus section transfers signals at a first speed;

said second bus section transfers signals at a second speed faster than said first speed;

faster signals from said second bus section transfer to said digital processor subsystem via said programmable logic core and said sharing unit; and

slower signals from said first bus section transfer to said digital processor subsystem via said bus interface and said sharing unit.

25. (New) For a first external device operating at a first speed and a second external device operating at a second speed, an integrated circuit for processing data from said first external device and data from said second external device, said integrated circuit comprising:

a bus subsystem having a first section adapted for coupling to said first external device and a second section adapted for coupling to said second external device, said first section of said bus subsystem coupled to said second section of said bus system;

a first programmable logic core coupled to said second section of said bus subsystem;

a second programmable logic core coupled to said second section of said bus subsystem;

a digital signal processor subsystem;

a first sharing unit;

a second sharing unit coupled to said first programmable logic core, said second programmable logic core and said first sharing unit, said second sharing unit adapted to alternately couple said first programmable logic core and said second programmable logic core to said first sharing unit;

said first sharing unit coupled to said digital signal processor, said bus subsystem and said second sharing unit, said second sharing unit adapted to alternately couple said first sharing unit and said bus subsystem to said digital signal processor;

wherein data from said first external device is transmitted to said digital processor subsystem via said first section of said bus subsystem and said first sharing unit; and

wherein data from said second external device is transmitted to said digital processor subsystem via said second section of said bus subsystem, one of said first or second programmable logic cores, said second sharing unit and said first sharing unit.

26. (New) An integrated circuit according to Claim 25, and further comprising:

a bridge, said bridge coupling said first section of said bus subsystem to said second section of said bus subsystem.

27. (New) An integrated circuit according to Claim 26, and further comprising:

a data buffer coupled to said first programmable logic core, said second programmable logic core and said second section of said bus subsystem, said data buffer adapted for receiving data from said second external device for subsequent transmission to said first and second programmable logic cores on a first-in-first-out basis.